REMARKS

Claims 1 and 4 are rejected under 35 U.S.C. §102(e) as being unpatentable over Yamauchi et al. (U.S. Patent No. 6,717,460) and claims 1-3 are rejected under U.S.C. 102(e) as being unpatentable over Matsumoto et al. (U.S. Patent No. 6,809,577). Claims 5-9 have been confirmed as reciting allowable subject matter. Claims 10-18 have been added by amendment above. No new matter has been added.

The present invention provides an internal voltage generating circuit. Claim 1, for example, recites an internal voltage generating circuit that includes an internal voltage-generating unit for converting an external power supply voltage into an internal voltage according to a reference voltage and outputting the internal voltage; and a plurality of internal voltage drop control units that are sequentially operated by enable signals, which are sequentially generated according to levels of the internal voltage, for stabilizing the internal voltage to a constant voltage level.

Meanwhile, Yamauchi et al. discloses that a current drive transistor (966) is operated by an output signal from comparison circuit (965), for stabilizing a periphery power supply line (965). Also, Matsumoto et al. discloses that a drive transistor (17) and P-channel transistor (19) are operated by an output signal from a comparator (13, 14, 15 and 16) and oscillation detection circuit (1), respectively, for stabilizing an internal power supply node (2).

In contrast, claim 1 recites a plurality of internal voltage drop control units. Accordingly, although the internal voltage cannot be boosted to a target voltage level due to the limit in a driving capability of one internal voltage drop control unit, remaining internal voltage drop control units are sequentially operated to boost the internal voltage to the target voltage level. The current driver of Yamauchi et al. and the current drive of Matsumoto et al., however, consist of only one current driver. Accordingly, if the current driver cannot be boosted to a target voltage level due to the limit in a driving capability of the current driver, the internal voltage cannot be boosted to a target voltage level. In any event, as none of the art of record teaches or suggests the claimed subject matter, the rejections of claim 1 and claims 2-9 are traversed.

With respect to claim 10, that claim recites a plurality of enable signal generating units for detecting a voltage level of the internal voltage and sequentially generating the enable signals. Yamauchi et al. and Matsumoto et al., however, do not teach or even suggest a plurality of enable signal generating units, as recited. *A fortiori*, they cannot be said to teach or suggest the subject matter recited in claim 10 or claims 11-18 depending therefrom.

Therefore, applicant believes that the amended claim 1 is patentable over the art of record and claims 2-9 depending from claim 1 are similarly in condition for allowance. Also, applicant believes that claim 10 is patentable over the art of record and claims 11-18 depending from the base claim 10 are similarly in condition for allowance. All pending claims (1-18) are in condition for immediate allowance.

Dated: March 10, 2005

Respectfully submitted,

By _____

Paul B. Stephens
Registration No.: 47,970
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant